REMARKS

Claims 1 – 7 are currently pending. New claim 8 has been added. Claims 1 – 3 have been allowed. Applicant respectfully requests reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claim 4 was rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,747,946 to Kaneko *et al.* (hereafter: "Kaneko"). Applicant respectfully requests that this rejection be withdrawn for the following reasons.

Claim 4 recites the novel embodiment disclosed, for example, on pgs. 7 – 8 of a method for effectively pruning a fast Fourier transform (FFT) circuit having a plurality of computational stages, each of which includes a plurality of butterfly modules, the method comprising: determining which butterfly modules need to be pruned for a particular application of the FFT circuit; and forcing the input signals of the butterfly modules located in the determining step to zero, whereby the selected butterfly modules are effectively pruned from the circuit because of their zero inputs.

Kaneko discloses an inverse fast Fourier transform device in which four information signal pieces are fed to the four terminals X[1], X[5], X[9], and X[13] among the frequency-domain input terminals X[0], X[1], X[2], . . . , and X[15], respectively. The other terminals among the frequency-domain input terminals X[0], X[1], X[2], . . . , and X[15] are connected to a ground, and are not subjected to information signal pieces. Thus, the IFFT device uses only 4 carriers (1st, 5th, 9th, and 13th carriers) among 16 carriers. The other carriers are unused or inactive. The results of IFFT calculations with respect to the four information signal pieces are outputted to the terminals x[0], x[1], x[2], . . . , and x[15]. The IFFT calculation results correspond to the 1st, 5th, 9th, and 13th carriers modulated in accordance with the four

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information signal pieces. The IFFT calculation results include sequences of signal samples representing output signal voltages. (See Col. 20, Lines 10 – 12).

However, Kaneko fails to disclose forcing input signals of the non-selected 16 carriers to zero. Rather, Kaneko discloses that the other terminals among the frequency-domain input terminals X[0], X[1], X[2], . . . , and X[15] are connected to a ground, and are not subjected to information signal pieces. That is, the other carriers are unused or inactive. No input signal on these terminals is forced to zero.

Therefore, because Kaneko fails to disclose forcing input signals of the non-selected 16 carriers to zero, it is respectfully requested that the rejection of claim 4 under 35 U.S.C. 102(e) be withdrawn.

Claims 5 – 7 were objected to for depending upon a rejected base claim. However, the Examiner stated that claims 5 – 7 would be allowable if amended to be in independent form including the limitations of the base claim. Applicant has accordingly amended claims 5 – 6 to be in independent form including the limitations of the base claim. Claim 7 depends from claim 6. Therefore, claims 5 – 7 should be in condition for allowance.

New claim 8 is presented for examination. New claim 8 recites *inter alia* forcing the input signals of the one or more butterfly modules located in stages subsequent to an initial stage to zero. In comparison, Kaneko discloses connecting terminals of an initial stage to ground. Also, as discussed above, Kaneko fails to disclose forcing input signals of the non-selected 16 carriers to zero. Therefore, new claim 8 should be in condition for allowance.

In view of the foregoing, the applicant submits that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the Examiner is invited to contact the undersigned by telephone.

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If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

Respectfully submitted,

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